IN THE CLAIMS

Claim 1. (Currently Amended) A semiconductor apparatus having a delay monitor circuit for monitoring critical path delay characteristics of a target circuit, wherein said delay monitor circuit comprises:

delay means having a plurality of delay elements for forming delay element arrays in accordance with supplied configuration information, wherein said delay means includes a delay component to cause a signal propagation delay in said target circuit;

a plurality of registers for setting therein a plurality of configuration information for forming said delay element arrays; and

switching means for selectively switching the configuration information of said plurality of registers and supplying the configuration information to said delay means;

wherein said configuration information indicates the number of stages of element arrays to fabricate the delay characteristics of a critical path of said target circuit.

Claim 2. (previously presented) The semiconductor apparatus as set forth in claim 10, wherein said switching means switches the configuration information of the delay element arrays set in the plurality of registers in a time sharing manner and supplies the configuration information to said delay means.

Claim 3. (previously presented) The semiconductor apparatus as set forth in claim 2, wherein said delay monitor

circuit comprises a control means for controlling a power source voltage supplied to said target circuit based on delay information generated by a delay element array formed in a time sharing manner.

Claim 4. (previously presented) The semiconductor apparatus as set forth in claim 3, wherein said control circuit compares a plurality of delay information generated by a plurality of delay element arrays formed in the delay means, judges a delay information with a largest delay value as a final delay information and controls said power source voltage based on the final delay information.

Claim 5. (Currently Amended) A semiconductor apparatus having a delay monitor circuit for monitoring critical path delay characteristics of a target circuit including a plurality of circuits operating at a plurality of different clock frequencies, wherein said delay monitor circuit comprises:

delay means having a plurality of delay elements for forming delay element arrays in accordance with supplied configuration information, wherein said delay means includes a delay component to cause a signal propagation delay in said target circuit;

a plurality of registers for setting therein a plurality of configuration information for forming said delay element arrays in accordance with said plurality of different clock frequencies;

first switching means for selectively switching the configuration information of said plurality of registers and supplying the configuration information to said delay means;

and

second switching means for selectively switching said plurality of different clock frequencies for supply to said delay means;

wherein said configuration information indicates the number of stages of element arrays to fabricate the delay characteristics of a critical path of said target circuit.

Claim 6. (previously presented) The semiconductor apparatus as set forth in claim 12, wherein:

said first switching means switches the configuration information of delay element arrays set to a plurality of registers in a time sharing manner and supplies the configuration information to said delay means; and

said second switching means switches said plurality of different clock frequencies in a time sharing manner for supply to said delay means

Claim 7. (previously presented) The semiconductor apparatus as set forth in claim 6, wherein said delay monitor circuit comprises a control means for controlling a power source voltage for supplying to said target circuit based on delay information generated by a delay element array formed in a time sharing manner.

Claim 8. (previously presented) The semiconductor apparatus as set forth in claim 7, wherein said control circuit compares a plurality of delay information generated by a plurality of delay element arrays formed in said delay means, and controls said

power source voltage based on a delay information with a largest delay ratio with respect to a clock cycle in a plurality of clock frequency domains.

Claim 9. (previously presented) The semiconductor apparatus as set forth in claim 8, wherein said plurality of registers have set therein a plurality of configuration information corresponding to the respective clock frequency domains.

Claim 10. (canceled)

Claim 11. (currently amended) The semiconductor apparatus as set forth in claim ~~10~~1, wherein said delay means has a plurality of delay elements having at least two delay components to cause signal propagation delay inside the target circuit.

Claim 12. (canceled)

Claim 13. (currently amended) The semiconductor apparatus as set forth in claim ~~12~~5, wherein said delay means has a plurality of delay elements having at least two delay components to cause signal propagation delay inside the target circuit.